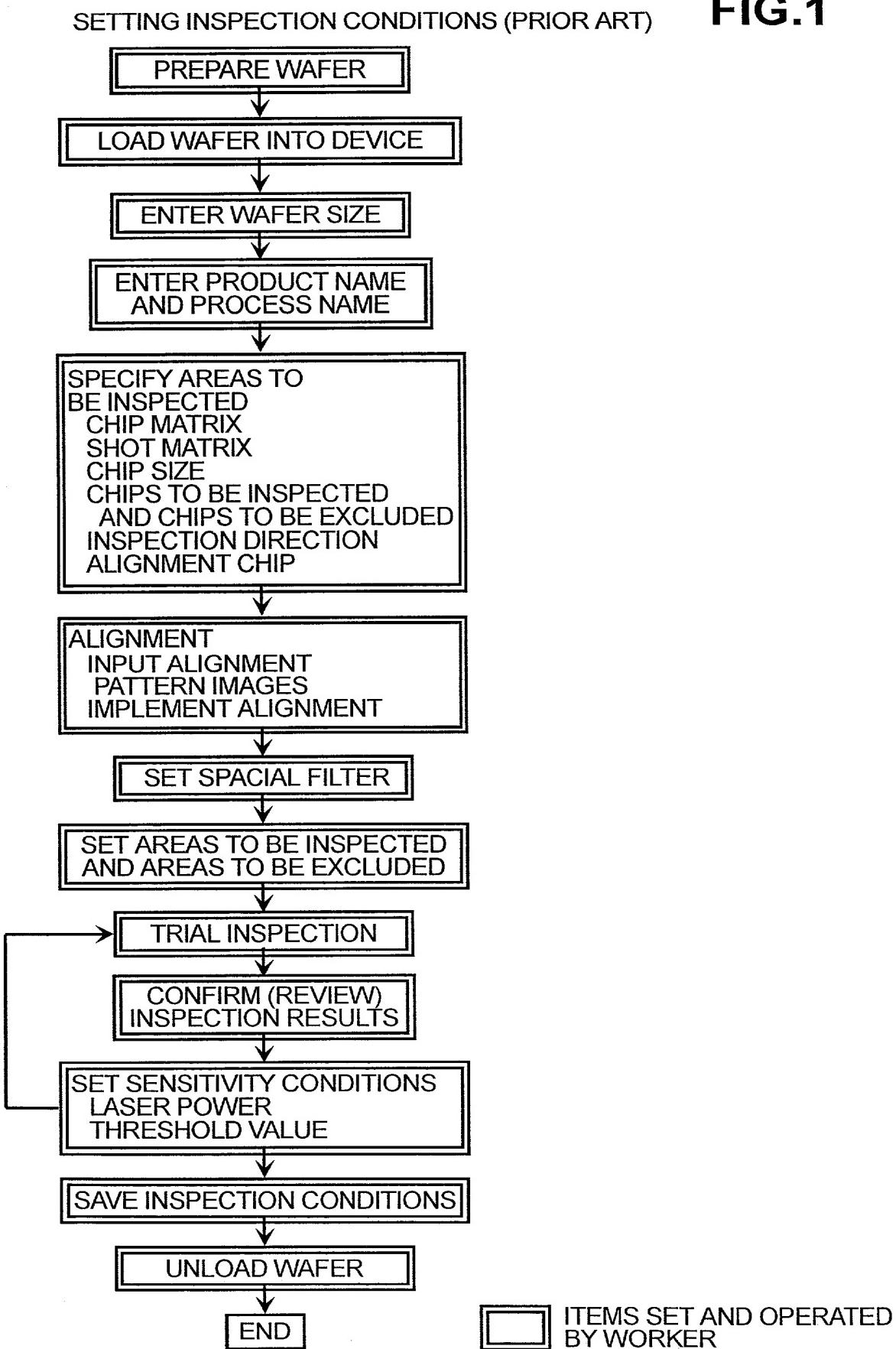


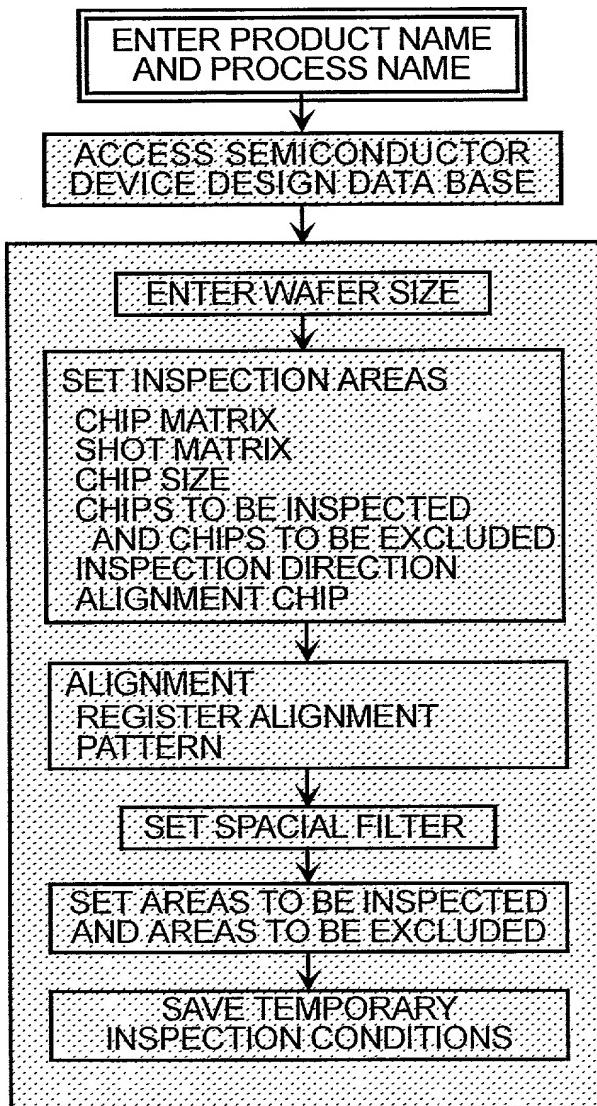
**FIG.1**



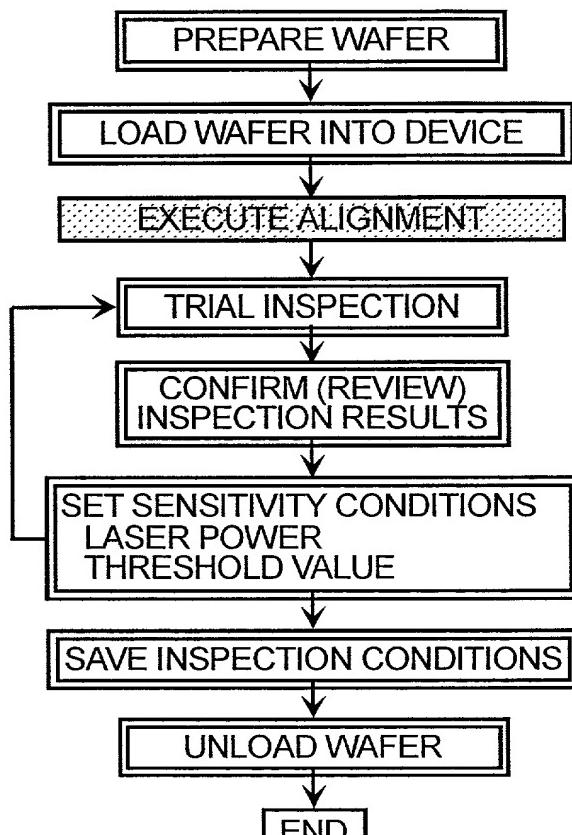
## FIG.2

### SETTING INSPECTION CONDITIONS

BEFORE WAFER ARRIVES



AFTER WAFER ARRIVES



ITEMS PROCESSED  
AUTOMATICALLY



ITEMS SET AND OPERATED  
BY WORKER

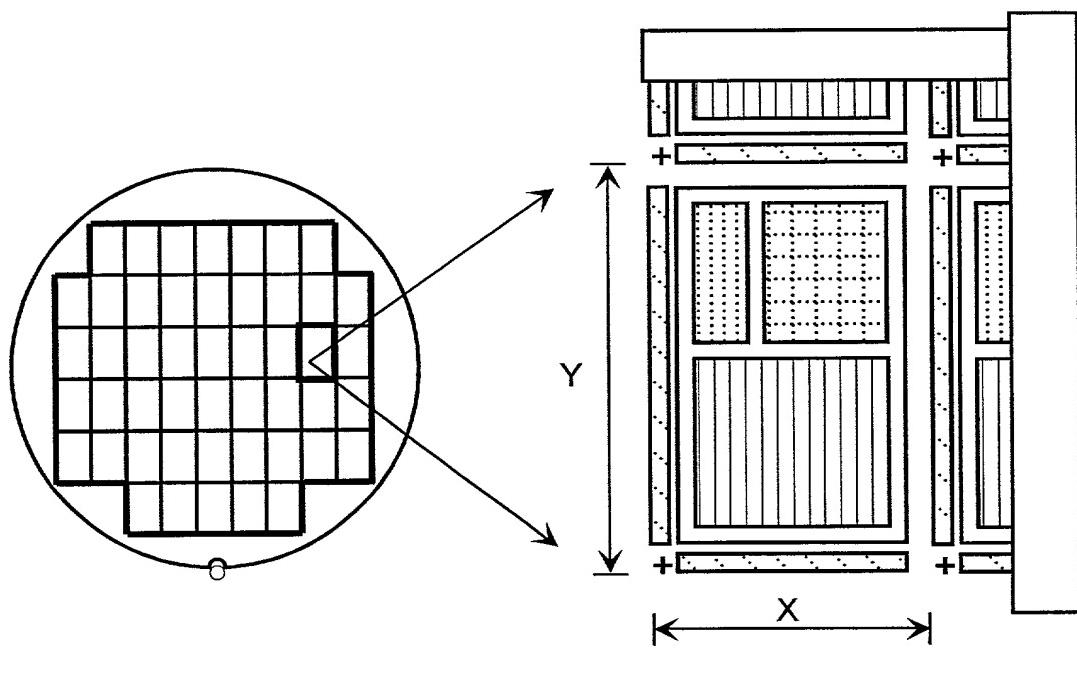
**Applicant:** Akira Hamamatsu, et al.

**Title:** Semiconductor Device Inspection Method

**Atty Docket No.** 16869P-041800

**Sheet 3 of 13**

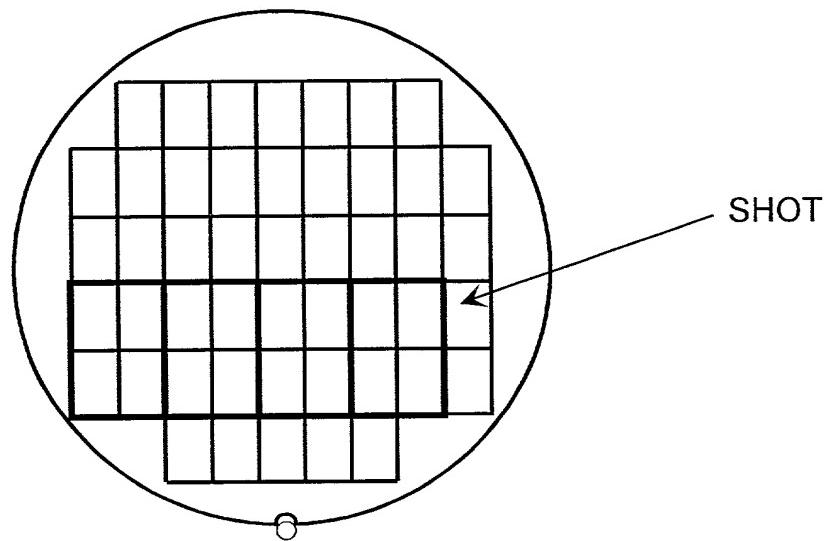
## FIG.3



SETTING CHIP SIZE

**Applicant:** Akira Hamamatsu, et al.  
**Title:** Semiconductor Device Inspection Method  
**Atty Docket No.** 16869P-041800  
**Sheet 4 of 13**

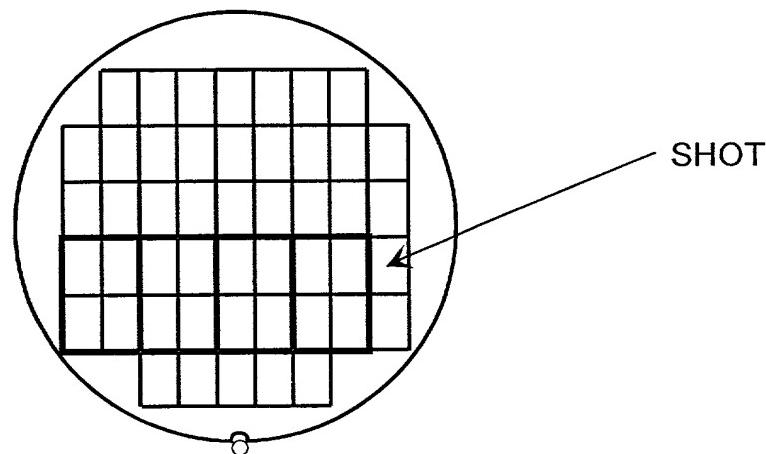
## FIG.4



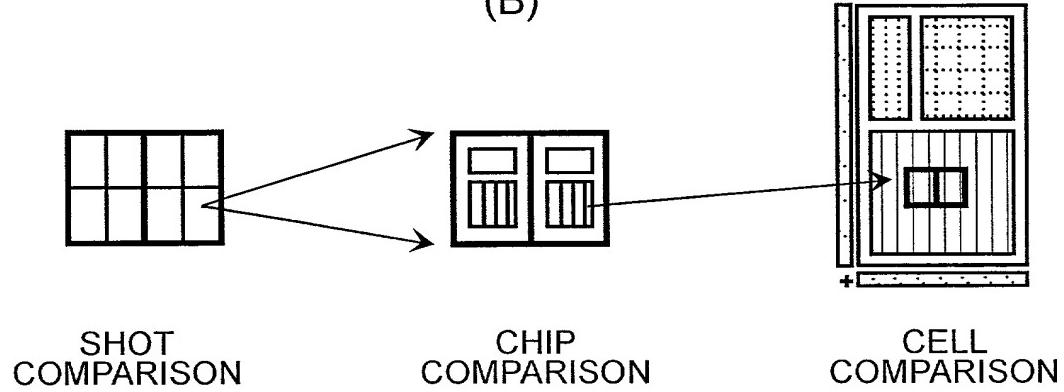
SETTING SHOT MATRIX

## FIG.5

(A)



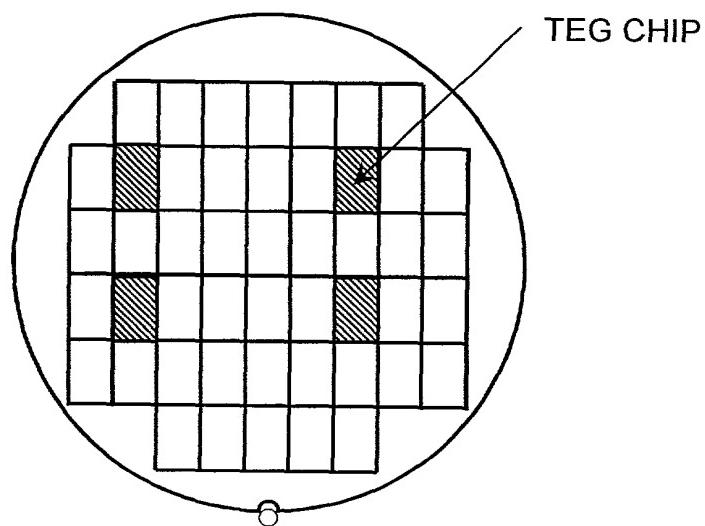
(B)



SET THE COMPARISON METHOD TO SUIT THE  
REPETITIVE UNIT

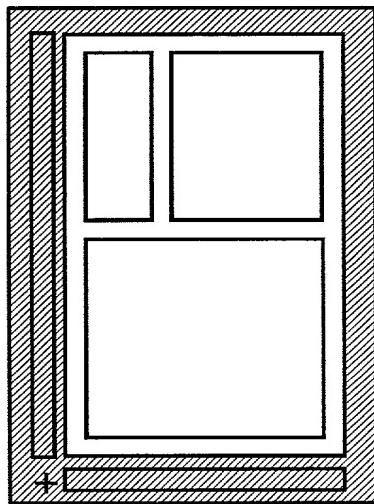
SETTING THE INSPECTION SEQUENCE

## FIG.6



SETTING CHIPS TO BE EXCLUDED  
FROM INSPECTION

## FIG.7



□ AREAS TO BE INSPECTED  
▨ AREAS EXCLUDED FROM  
INSPECTION (SCRIBE AREA)

SETTING AREAS TO BE INSPECTED  
AND AREAS TO BE EXCLUDED

## FIG.8



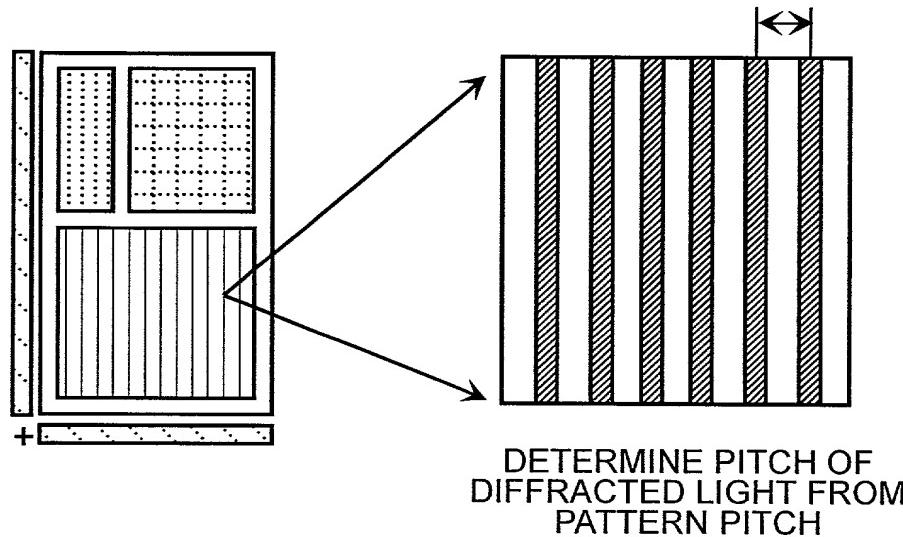
SELECT PATTERNS AND MATERIAL  
THAT WILL MAKE IMAGES EASILY  
RECOGNISABLE DURING ALIGNMENT

SETTING THE  
ALIGNMENT PATTERN

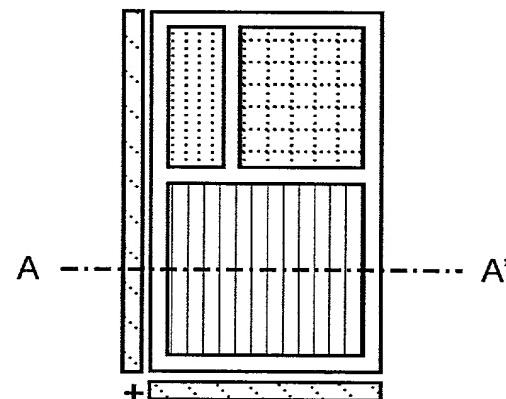
## FIG. 9

(A)

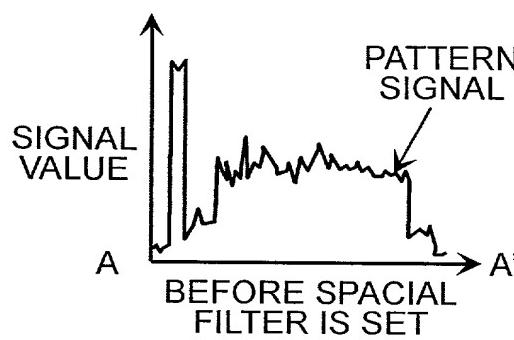
PATTERN PITCH:  $d$



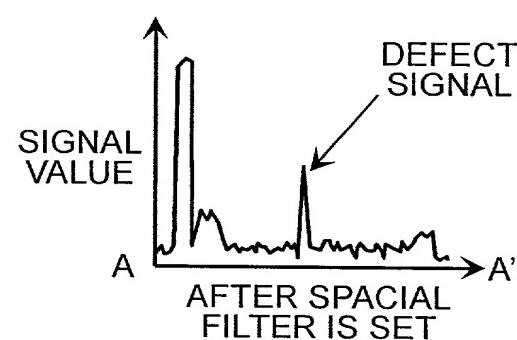
(B)



(C)



(D)



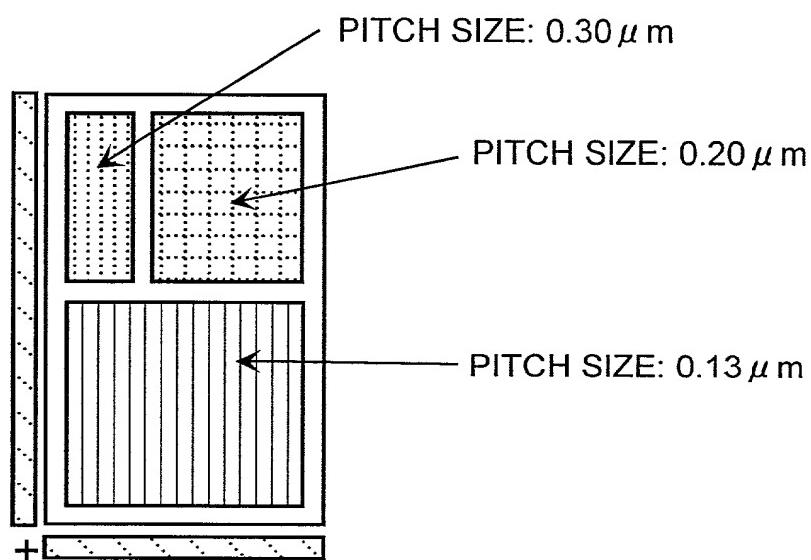
**Applicant:** Akira Hamamatsu, et al.

**Title:** Semiconductor Device Inspection Method

**Atty Docket No.** 16869P-041800

**Sheet 9 of 13**

## FIG.10



**FATALITY JUDGEMENT  
(BY PRODUCT, PROCESS, AND AREA)**

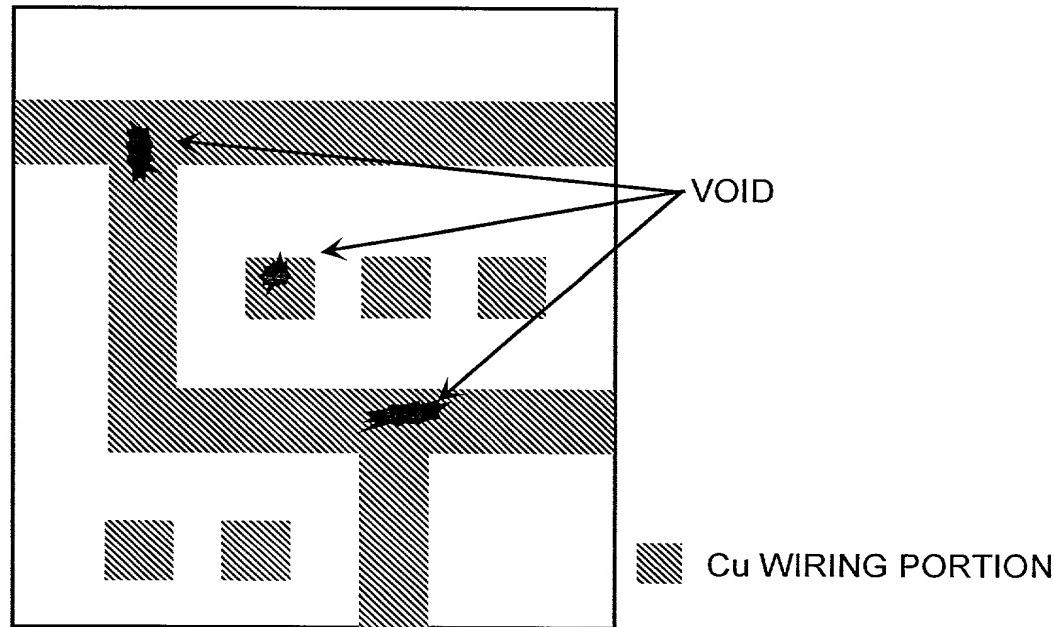
**Applicant:** Akira Hamamatsu, et al.

**Title:** Semiconductor Device Inspection Method

**Atty Docket No.** 16869P-041800

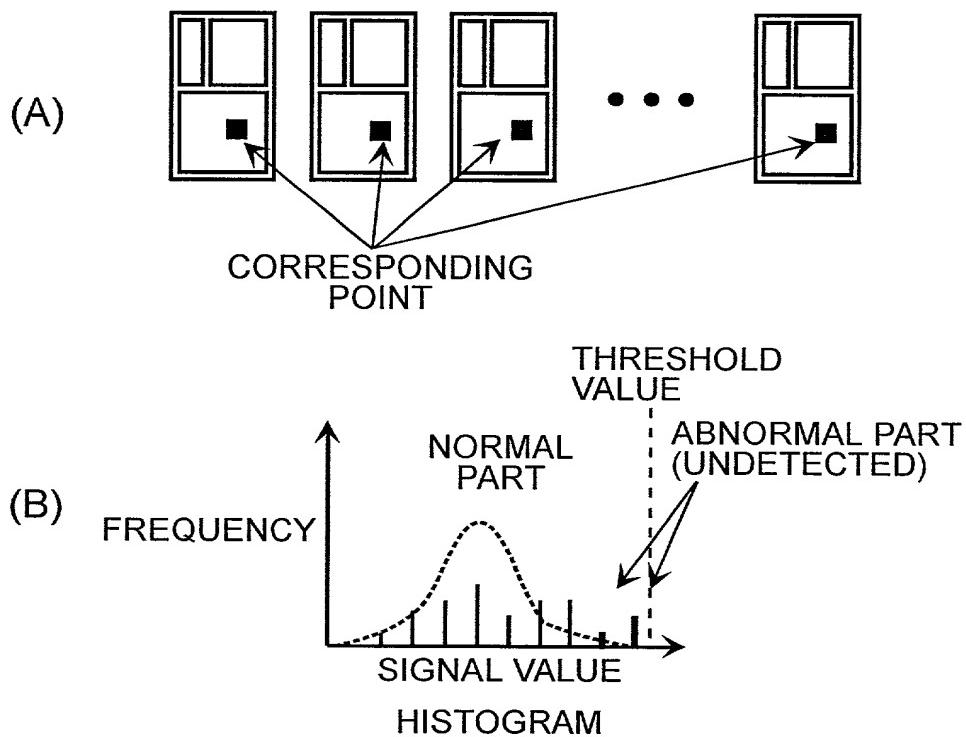
**Sheet 10 of 13**

## FIG.11

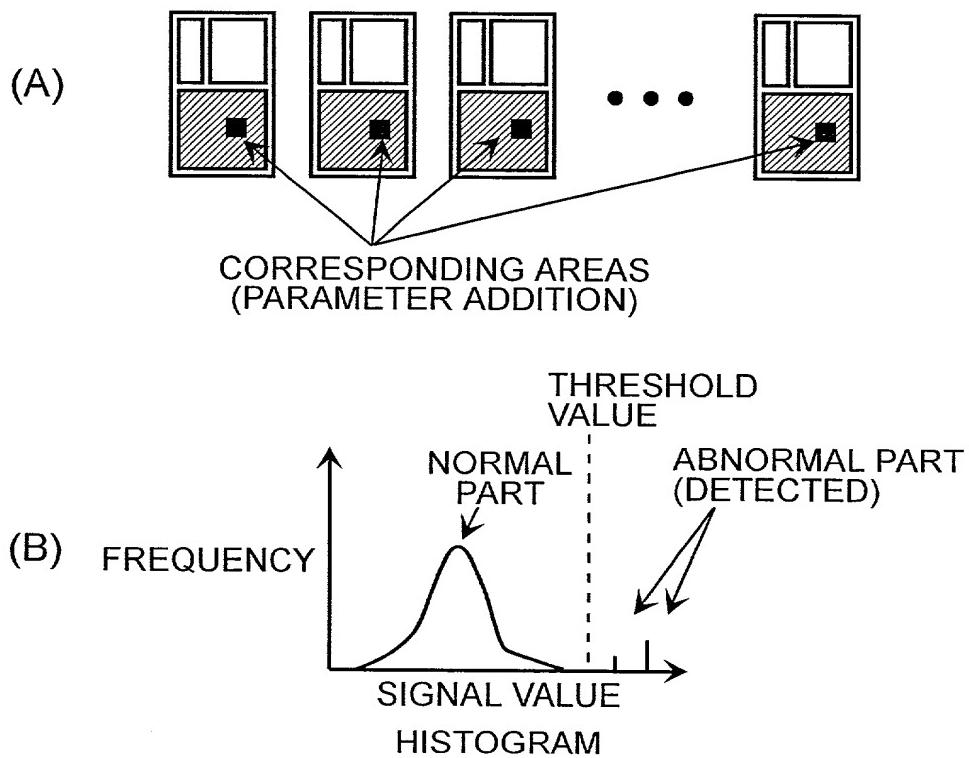


AUTOMATIC DEFECT CLASSIFICATION  
TECHNOLOGY

## FIG.12



## FIG.13



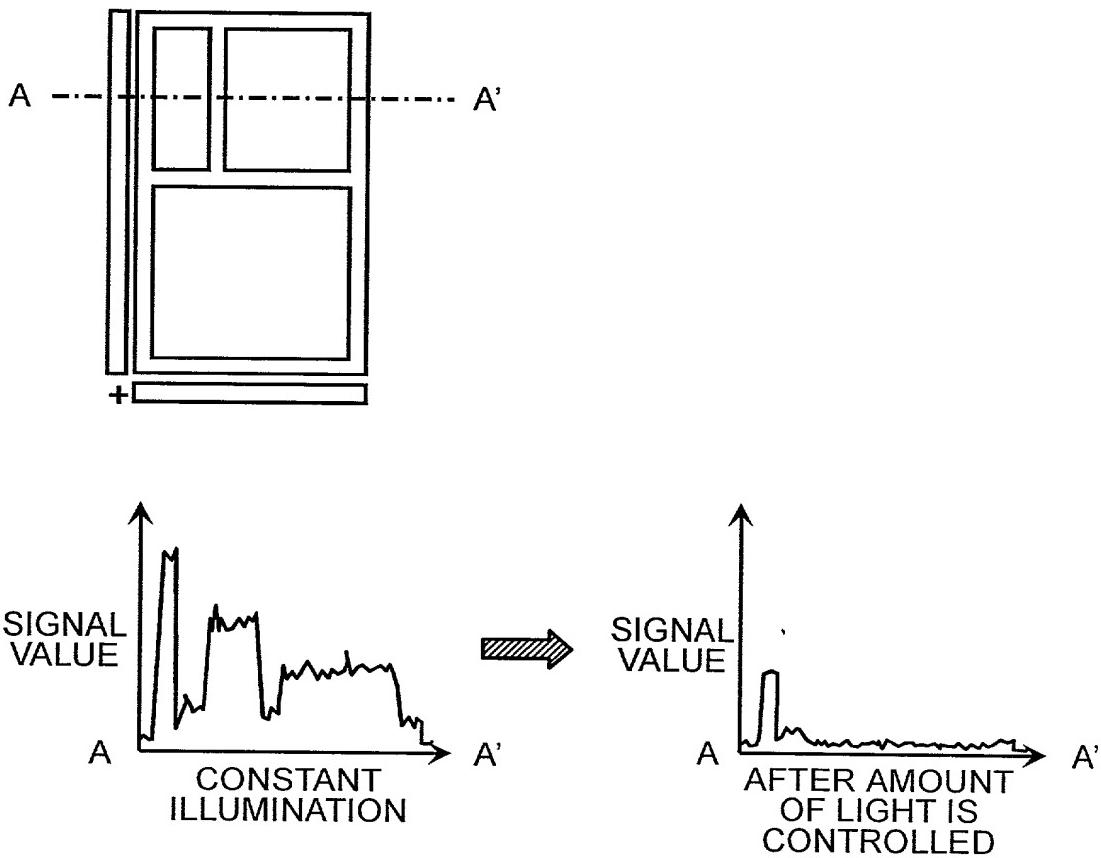
Applicant: Akira Hamamatsu, et al.

Title: Semiconductor Device Inspection Method

Atty Docket No. 16869P-041800

Sheet 12 of 13

## FIG.14



ESTIMATE THE SIGNAL INTENSITY FROM PATTERN  
PITCH AND CONTROL THE AMOUNT OF LIGHT

SETTING THE AMOUNT OF LIGHT

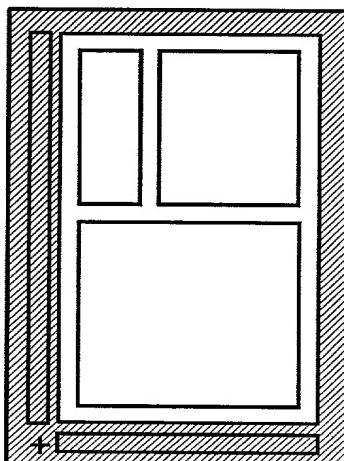
**Applicant:** Akira Hamamatsu, et al.

**Title:** Semiconductor Device Inspection Method

**Atty Docket No.** 16869P-041800

**Sheet 13 of 13**

## FIG.15



[diagonal hatching] AREAS IN WHICH MANY FALSE ALARMS OCCUR  
[brace] SCRIBE AREA AROUND MEMORY MAT

SETTING AREAS IN WHICH MANY FALSE ALARMS OCCUR